REMARKS

Claims 1-27 and 29 are currently pending in the present application.

(1) The Office Action rejected claims 1-4, 7, 9, 14, 16 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Lee, U.S. Patent No. 6,759,335 ("Lee") in view of Stamp et al., U.S. Patent Publication No. 2004/0084149 ("Stamp"). The Office Action rejected claims 5, 6, 8, 10-13 and 18-24 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Stamp and Chung et al., U.S. Patent No. 6,734,106 ("Chung"). The Office Action rejected claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Stamp and Cheong, U.S. Patent Publication No. 2003/0186533 ("Cheong"). The Office Action rejected claims 25-27 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Stamp and Chung and Cheong. Applicant respectfully traverses these rejections.

Firstly, Applicant asserts that Lee and Stamp cannot be combined in the manner proposed by the Office Action. "If [the] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." M.P.E.P. § 2143.01(V) (citing In re Gordon, 733 F.2d 900 (Fed. Cir. 1984)). In particular, it is not clear how Stamp's silicon-containing film 410 of Fig. 4A can be functionally incorporated as Lee's buried strap 62 of Figs. 6-7 as proposed by the Office Action. Stamp, on the one hand, discloses that silicon-containing film 410 exhibits good step coverage, which Stamp describes as uniform film thickness across different step heights of the conformal silicon-containing film. *See, e.g.*, Stamp, ¶ [0061], Fig. 4.

Lee, on the other hand, discloses depositing polysilicon buried strap 62 using a selective deposition method such as a hemispherical grain (HSG) process. *See, e.g.*, Lee, Fig. 6, col. 3:61-col. 4:7. As taught by Lee, the "selective hemispherical grain (HSG) polysilicon deposition scheme is used to deposit a controlled thickness of polysilicon over an amorphous silicon layer. The process of the present invention controls buried strap thickness and doping level." *Id.* at col. 2:50-54. Unlike the conformal step coverage taught by Stamp, Lee teaches selectively forming buried strap 62 essentially only on amorphous silicon 54. *See id.* at col. 3:61-col. 4:7, Fig. 6. Substituting the uniform, conformal silicon-containing film 410 of Stamp for Lee's buried strap 62 would form a silicon-containing layer non-selectively deposited on essentially all exposed surfaces, not just on amorphous silicon 54. Because this would render the device of Lee unsatisfactory for its intended purpose, Applicant asserts that there is no motivation for one of ordinary skill in the art to make the proposed combination.

Secondly, a "prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." M.P.E.P. § 2141.02(VI) (citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)) (emphasis in original). The Office Action states that it would have been obvious to modify Lee with Stamp to provide good step coverage over the trench in the semiconductor substrate. *See* Office Action, p. 3 (citing Stamp, ¶ [0061]). Lee, however, discloses selective deposition and teaches away from "good step coverage." For example, Lee states that the "selective HSG polysilicon deposition method deposits the buried strap polysilicon to a controlled thickness. This process avoids planarization of the buried strap layer by CMP which adds process

complexity." Lee, col. 4:20-24. Substituting in Stamp's conformal silicon-containing layer, if workable at all, would require the very planarization that Lee is seeking to avoid with the selective deposition process. Thus, Lee teaches away from using a conformal step coverage process, such as that of Stamp, because it would add process complexity.

Accordingly, Applicant respectfully submits that Stamp cannot be combined with Lee, and therefore submits claims 1-17 and 18-27 are patentable over the cited prior art.

(2) The Office Action rejected claim 29 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Mo, U.S. Patent Publication No. 2002/0024091 ("Mo"). Applicant respectfully traverses this rejection.

Firstly, Applicant asserts that Lee and Mo cannot be combined in the manner proposed by the Office Action. "If [the] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." M.P.E.P. § 2143.01(V) (citing In re Gordon, 733 F.2d 900 (Fed. Cir. 1984)). In particular, it is not clear how Mo's conformal polysilicon layer 614 of Fig. 6B can be functionally incorporated as Lee's buried strap 62 of Figs. 6-7 as proposed by the Office Action. Mo, on the one hand, shows that polysilicon layer 614 is conformal and uniform, providing good step coverage across the substrate. *See, e.g.*, Lee, Figs. 6B-6C.

Lee, on the other hand, discloses depositing polysilicon buried strap 62 using a selective deposition method such as a hemispherical grain (HSG) process. *See, e.g.*, Lee, Fig. 6, col. 3:61-col. 4:7. As taught by Lee, the "selective hemispherical grain (HSG) polysilicon deposition scheme is used to deposit a controlled thickness of polysilicon over an amorphous silicon layer. The process of the present invention controls buried

strap thickness and doping level." *Id.* at col. 2:50-54. Unlike the conformal step coverage taught by Mo, Lee teaches selectively forming buried strap 62 essentially only on amorphous silicon 54. *See id.* at col. 3:61-col. 4:7, Fig. 6. Substituting the uniform, conformal polysilicon layer 614 of Mo for Lee's buried strap 62 would form a polysilicon layer non-selectively deposited on essentially all exposed surfaces, not just on amorphous silicon 54. Because this would render the device of Lee unsatisfactory for its intended purpose, Applicant asserts that there is no motivation for one of ordinary skill in the art to make the proposed combination.

Secondly, a "prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." M.P.E.P. § 2141.02(VI) (citing W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)) (emphasis in original). The Office Action states that it would have been obvious to modify Lee with Mo to provide good step coverage over the trench in the semiconductor substrate. *See* Office Action, p. 12 (citing Stamp, ¶ [0061]). Lee, however, discloses selective deposition and teaches away from "good step coverage." For example, Lee states that the "selective HSG polysilicon deposition method deposits the buried strap polysilicon to a controlled thickness. This process avoids planarization of the buried strap layer by CMP which adds process complexity." Lee, col. 4:20-24. Substituting in Mo's conformal polysilicon layer, if workable at all, would require the very planarization that Lee is seeking to avoid with the selective deposition process. Thus, Lee teaches away from using a conformal step coverage process, such as that of Mo, because it would add process complexity.

Accordingly, Applicant respectfully submits that Mo cannot be combined with Lee, and therefore submits claim 29 is patentable over the cited prior art.

In view of the above, Applicant respectfully submits that this response complies with 37 C.F.R. § 1.116. Applicant further submits that the claims are in condition for allowance. No new matter has been added by this response. If the Examiner should have any questions, please contact Applicant's Attorney, Brian A. Carlson, at 972-732-1001. The Commissioner is hereby authorized to charge any fees due in connection with this filing, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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